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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,549	01/23/2002	Akihiko Ebina	111779	4562

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EXAMINER	
PIZARRO CRESPO, MARCOS D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,549	EBINA ET AL.	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Attorney's Docket Number: 111779
Filing Date: 1/23/2002
Claimed Foreign Priority Date: 1/30/2001 (JP 2001-21930)
Applicant(s): Ebina et al.
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to amendment in paper no. 7 filed on 3/3/2003.

Acknowledgment

1. The amendment in paper no. 7, filed on 3/3/2003, in response to the Office action in paper no. 6, mailed on 12/3/2002, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-19.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 6-8, 10, 11, 13, 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Seiki (US 6248633).

5. Seiki shows (see, *e.g.*, fig. 4A-4G) all aspects of the instant invention including a semiconductor IC device having a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix with a plurality of rows and columns, wherein each of the memory devices comprises:

- a word gate **245** formed on a semiconductor layer **200** with a first gate insulating layer **221** interposed
- an impurity diffusion layer **204** which forms either a source or a drain region
- first and second control gates **240** in the shape of sidewalls formed along either side of the word gate **245**

wherein:

- the first control gate **240** is disposed on the semiconductor layer **200** with a second gate insulating layer **230** interposed, and also on the word gate **245** with a side insulating layer **234** interposed
- the second control gate **240** is disposed on the semiconductor layer **200** with another second gate insulating layer **230** interposed, and also on the word gate **245** with another side insulating layer **234** interposed
- the first and second control gates **240** extend in a first direction (see, *e.g.*, fig.4G)

- a pair of the first and second control gates **240**, adjacent in a second direction which intersects the first direction, is connected to a common contact section (see, *e.g.*, figs. 4E and 7A)

6. Regarding claim 2, Seiki shows (see, *e.g.*, fig. 4G) that each of the first and second control gates **240** is formed of a conductive layer extending in the direction in which the impurity diffusion layer **204** extends.

7. Regarding claim 3, Seiki shows (see, *e.g.*, fig. 4F) that the common section is connected to the first and second control gates **240** and may include a conductive layer **247** formed of the same material as the first and second control gates **240**.

8. Regarding claim 4, Seiki shows (see, *e.g.*, fig. 4F) that the common contact section includes an insulating layer **235** formed on the semiconductor layer **200**, a conductive layer **247** formed on the insulating layer **235**, and a cap layer **236** formed on the conductive layer **247**.

9. Regarding claim 6, Seiki shows (see, *e.g.*, fig. 4F) that the side insulating layers **234** are located between the word gate **245** and the first and second control gates **240**. In addition, Seiki shows that the upper ends of the side insulating layers **234** are located higher than the first and second control gates **240** with respects to the semiconductor layer **200**.

10. Regarding claim 7, Seiki shows (see, *e.g.*, fig. 4F) a buried insulating layer **247** disposed between two side insulating layers **234** in contact with first and second control gates **240**. The buried insulating layer **247** covers adjacent first and second control gates **240**.

11. Regarding claim 8, Seiki shows (see, *e.g.*, fig. 4E) the common contact section in contact with one end of the impurity diffusion layer **204**.

12. Regarding claim 10, Seiki shows (see, *e.g.*, fig. 4G) the memory cell array divided into a plurality of blocks. In addition, Seiki shows (see, *e.g.*, fig. 4G) that the impurity diffusion layers **204** in blocks adjacent to each other in the first direction are connected to each other through a contact impurity diffusion layer formed in the semiconductor layer **200**.

13. Regarding claim 11, Seiki (col.5/ll.7) shows that the second gate insulating layer **230** is formed of a laminate consisting of a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.

14. Regarding claim 13, Seiki shows (see, *e.g.*, figs. 4A-4G) all aspects of the instant invention including a semiconductor integrated circuit device having a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix with a plurality of rows and columns, each of the memory devices comprising:

- a word gate **245** formed on the semiconductor layer **200** with a first gate insulating layer **221** therebetween
- an impurity diffusion layer **204** which forms either a source region or a drain region
- a first control gate **240** formed along a first side of the word gate **245** and on the semiconductor layer **200**
- a second gate insulating layer **230** between the first control gate **240** and the semiconductor layer **200**

- a side insulating layer **234** between the first control gate **240** and the first side of the word gate **245**
- a second control gate **240** formed along a second side of the word gate **245** and on the semiconductor layer **200**
- another second gate insulating layer **230** between the second control gate **240** and the semiconductor layer **200**
- another side insulating layer **234** between the second control gate **240** and the second side of the word gate **245**

wherein:

- the first and second control gates **240** extend in a first direction (see, *e.g.*, fig. 4G)
- an end of a first control gate **240** and an end of a second control gate **240** that are adjacent to each other in a second direction which intersects the first direction, being connected to a common contact section (see, *e.g.*, fig. 4E, 7A)

15. Regarding claim 14, Seiki shows the first and second control gates **240** formed in the shape of sidewalls along either side of the word gate **245** (see, *e.g.*, fig. 4E).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 5, 12, and 15, are rejected under 35 U.S.C. 103(a) as being unpatentable over Seiki in view of Wang (US 6091101).

18. Regarding claims 5 and 15, Seiki shows (see, *e.g.*, fig. 4F) that the common contact section includes an insulating layer **235** formed on the semiconductor layer **200**. In addition, Seiki (col.5/ll.56) shows that the insulating layer **235** may be formed of a laminate consisting of a first silicon oxide layer and a silicon nitride layer, but fails to show an additional second oxide layer.

Nonetheless, as taught by Wang (col.2/ll.34-37), ONO dielectric layers are well known in the art for their superior insulating properties.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to included a second oxide layer in Seiki's insulating layer, as suggested by Wang, to improve its insulating properties.

19. Regarding claim 12, Seiki shows most aspects of the instant invention (see paragraphs 5-15 above). Seiki (col.4/ll.53) also shows that the side insulating layer **234** may be formed of a first oxide layer and a silicon nitride layer, but fails to show a second silicon oxide layer for the side insulating layer.

Nonetheless, as taught by Wang (col.2/ll.34-37), ONO dielectric layers are well known in the art for their superior insulating properties.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to included a second oxide layer in Seiki's side insulating layer, as suggested by Wang, to improve its insulating properties.

20. Claims 9 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seiki in view of Tsaur (US 4372031).

21. Regarding claims 9 and 16, Seiki shows most aspects of the instant invention (see paragraphs 5-15 above).

22. Regarding claim 17, Seiki shows a semiconductor integrated circuit device having a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix with a plurality of rows and columns, wherein each of the memory devices comprises:

- a word gate **245** formed on a semiconductor layer **200** with a first gate insulating layer **221** therebetween
- an impurity diffusion layer **204** that forms either a source region or a drain region
- first and second control gates **240** formed along either side of the word gate **245** in the shape of sidewalls

wherein:

- the first control gate **240** is disposed on the semiconductor layer **200** with a second gate insulating layer **230** therebetween, and also on the word gate **245** with a side insulating layer **234** therebetween
- the second control gate **240** is disposed on the semiconductor layer **200** with another second gate insulating layer **230** therebetween, and also on the word gate **245** with another side insulating layer **234** therebetween

- the first and second control gates **240** extend in a first direction (see, *e.g.*, fig. 4G)
- an end of the first control gate **240** and an end of the second control gate **240** of a pair of gates adjacent to each other in a second direction, which intersects the first direction, is connected to a common contact section (see, *e.g.*, fig. 7A)

23. Regarding claim 18, Seiki shows most aspects of the instant invention including a semiconductor integrated circuit device having a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix with a plurality of rows and columns, where each of the memory devices comprises:

- a word gate **245** formed on a semiconductor layer **200** with a first gate insulating layer **221** therebetween
- an impurity diffusion layer **204** which formed either a source region or a drain region
- first and second control gates **240** in the shape of sidewalls formed along either side of the word gate **245**

wherein:

- the first control gate **240** is disposed on the semiconductor layer **200** with a second gate insulating layer **230** therebetween, and also on the word gate **245** with a side insulating layer **234** therebetween
- the second control gate **240** is disposed on the semiconductor layer **200** with another second gate insulating layer **230** therebetween, and also on the word gate **245** with another side insulating layer **234** therebetween

- the first and second control gates **240** extend in a first direction (see, *e.g.*, fig. 4G)
- a pair of the first and second control gates **240**, adjacent in a second direction, which intersects the first direction, is connected to a common contact section (see, e.g., fig. 7A)

24. Regarding claims 9 and 16-18, Seiki (see, *e.g.*, fig. 7A) fails to show common contact sections that are staggered with respect to each other.

Tsaur (col.2/ll.67-col.3/ll.2), on the other hand, teaches that common contact sections with a staggered layout will increase the density of Seiki's cell array.

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to provide Seiki's common contact sections with a staggered layout, as suggested by Tsaur, to increase the density of the cell array.

25. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seiki in view of Tsaur (US 4372031) in view of Wang.

26. Regarding claim 19, Seiki/Tsaur shows most aspects of the instant invention (see paragraphs 21-24 above). In addition, see the comments stated above in paragraph 18 and with regards to claims 5 and 15, which are considered repeated here.

Response to Arguments

27. The applicants argue:

> Seiki fails to disclose first and second control gates that extend in a first direction; and an end of the first control gate and an end of the second control gate that are adjacent to each other in a second direction which intersects the first direction, being connected to a common contact section.

The examiner responds:

Opposing applicants' argument, Seiki shows the features that the applicants indicate. See, *e.g.*, fig. 4G, where Seiki clearly shows the first and second control gates **240** extending in a first direction. See also, *e.g.*, fig. 7A, where Seiki clearly shows that an end of a first control gate and an end of a second control gate that are adjacent to each other in a second direction, which intersects the first direction, is connected to a common contact section.

28. The applicants argue:

> Wang fails to teach that the insulating layer of the common contact section is formed of a laminate consisting of a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.

The examiner argues:

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In the instant case, Seiki shows (see, *e.g.*, fig. 4F) that the common contact section includes an insulating layer **235** formed on the semiconductor layer **200**. Seiki (col.5/ll.56) also shows that the insulating layer **235** may be formed of a laminate consisting of a first silicon oxide layer and a silicon nitride layer, but fails to show an additional second oxide layer.

Nonetheless, as taught by Wang (col.2/ll.34-37), ONO dielectric layers are well known in the art for their superior insulating properties.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to included a second oxide layer in Seiki's insulating layer, as suggested by Wang, to improve its insulating properties.

Conclusion

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

30. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

31. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and

between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

33. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

34. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/314,316,319,324,326,365,368,390,401,637,640,900	4/5/2003
Other Documentation: PLUS Analysis	11/21/02
Electronic Database(s): EAST (USPAT, EPO, JPO, PGPub)	4/5/2003

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MDP/mdp
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